1. A method of connecting an integrated circuit die to a substrate, comprising:

identifying a block of circuitry to be disabled within the integrated circuit die;

applying a pattern of solder bumps to one of the die and the substrate, the pattern of solder bumps excluding at least one solder bump used for connection to the block of circuitry;

placing the integrated circuit die on the substrate with solder pads on the die aligned with corresponding solder pads on the substrate and with the pattern of solder bumps disposed between the die and the substrate; and

heating the solder bumps to cause the solder to flow and form electrical connections between the substrate and the die.

2. The method according to claim 1, wherein the excluded solder bump, if present, would convey power supply voltage to the block of circuitry.

3. The method in accordance with claim 1, wherein the applying is carried out by applying solder through a mask selected in accordance with the block of circuitry to be disabled.

4. The method according to claim 1, wherein the identifying is carried out by testing blocks of circuitry for functionality, and wherein the block of circuitry to be disabled is determined to not be functional.

5. The method according to claim 1, wherein the identifying is carried out by determining that a specified performance criterion is required.

6. The method according to claim 1, wherein the block of circuitry to be disabled comprises one of a plurality of microprocessor cores.

7. The method according to claim 1, wherein the block of circuitry to be disabled comprises one of a plurality of memory blocks.

8. The method according to claim 1, wherein the block of circuitry to be disabled comprises one of a plurality of redundant blocks of circuitry.

9. The method according to claim 1, wherein the applying further comprises, applying a solder bump used to connect ground to the block of circuitry to be disabled.

10. A method of applying solder bumps for soldering a substrate to an integrated circuit die, comprising:

identifying a block of circuitry on the integrated circuit die that is to be disabled; and

applying a pattern of solder bumps to one of the die and the substrate, the pattern of solder bumps excluding at least one solder bump used for connection to the block of circuitry that is to be disabled.

11. The method according to claim 10, wherein the excluded solder bump, if present, would convey power supply voltage to the block of circuitry.

12. The method in accordance with claim 10, wherein the applying is carried out by applying solder through a mask selected in accordance with the block of circuitry to be disabled.

13. The method according to claim 10, wherein the identifying is carried out by testing blocks of circuitry for functionality, and wherein the block of circuitry to be disabled is determined to not be functional.

14. The method according to claim 10, wherein the identifying is carried out by determining that a specified performance criterion is required.

15. The method according to claim 10, wherein the block of circuitry to be

disabled comprises one of a plurality of microprocessor cores.

16. The method according to claim 10, wherein the block of circuitry to be disabled comprises one of a plurality of memory blocks.

17. The method according to claim 10, wherein the block of circuitry to be disabled comprises one of a plurality of redundant blocks of circuitry.

18. The method according to claim 10, wherein the applying further comprises, applying a solder bump used to connect ground to the block of circuitry to be disabled.

19. A method of configuring functionality of an integrated circuit die, comprising:

identifying a block of circuitry to be configured by selectively making an electrical connection between a substrate and the integrated circuit die;

applying a pattern of solder bumps to one of the die and the substrate, the pattern of solder bumps selectively excluding at least one solder bump used for connection to the block of circuitry;

placing the integrated circuit die on the substrate with solder pads on the die aligned with solder pads on the substrate and the pattern of solder bumps disposed therebetween; and

heating the solder bumps to cause the solder to flow and form electrical connections between the substrate and the die.

20. The method according to claim 19, wherein the excluded solder bump, if present, would convey power supply voltage to the block of circuitry.

21. The method according to claim 19, wherein the excluded solder bump, if present, would convey a signal as an input to a logic circuit in the block of circuitry.

22. The method in accordance with claim 19, wherein the applying is carried out by applying solder through a mask selected in accordance with the block of circuitry to be disabled.

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23. An integrated circuit device, comprising:

an integrated circuit die having a plurality of solder pads used for conveying signals to and from the die, the integrated circuit having a plurality of blocks of circuitry;

a substrate having a plurality of solder pads corresponding to at least a portion of the integrated circuit die's solder pads;

a plurality of solder bumps connecting the substrate to the integrated circuit die; and

wherein at least one of the blocks of circuitry is configured by virtue of omission of a solder bump for at least one connection between the substrate and the at least one of the plurality of blocks of circuitry.

24. The apparatus according to claim 23, wherein the one of the plurality of blocks of circuitry is disabled by omission of a solder bump that supplies power supply voltage to the at least one of the block of circuitry.

25. The apparatus according to claim 24, wherein the block of circuitry that is disabled is identified by testing the plurality of blocks of circuitry for functionality.

26. The apparatus according to claim 24, wherein the block of circuitry that is disabled is determined to not be functional by said testing.

27. The apparatus according to claim 24, wherein the block of circuitry that is disabled comprises one of a plurality of microprocessor cores.

28. The apparatus according to claim 24, wherein the block of circuitry that is disabled comprises at least one of a plurality of memory blocks.

29. The apparatus according to claim 24, wherein the block of circuitry that is disabled comprises one of a plurality of redundant blocks of circuitry.

30. The apparatus according to claim 24, wherein one of the plurality of solder bumps connects the substrate to a ground node in the block of circuitry that is disabled.

31. The apparatus according to claim 23, wherein the omitted solder bump, if present, would connect the substrate to a logic input forming a part of the block of circuitry.

32. The apparatus according to claim 23, wherein the substrate forms part of a chip carrier.

33. The apparatus according to claim 23, wherein the one of the plurality of blocks of circuitry is configured by selective connection of a signal to a logic gate.